ABSTRACT

The present invention pertains to formation of a transistor in a manner that mitigates parasitic capacitance, thereby facilitating, *inter alia*, enhanced switching speeds. More particularly, a sidewall spacer formed upon a semiconductor substrate adjacent a conductive gate structure includes a material having a low dielectric constant (low-k) to mitigate parasitic capacitance between the gate structure, the sidewall spacer and a conductive drain formed within the semiconductor substrate. The low-k sidewall spacer is encapsulated within a nitride material which is selective to etchants such that the spacer is not altered during subsequent processing. The spacer thus retains its shape and remains effective to guide dopants into desired locations within the substrate.